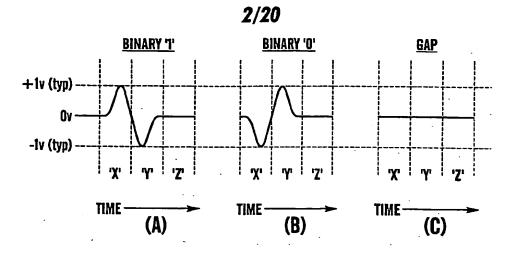
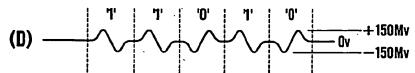
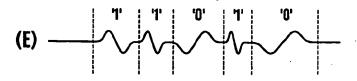
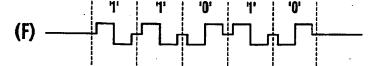


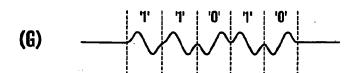
Fig. 1

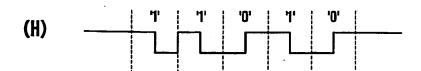












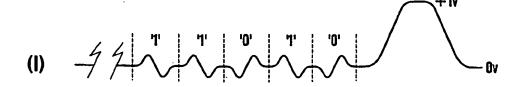
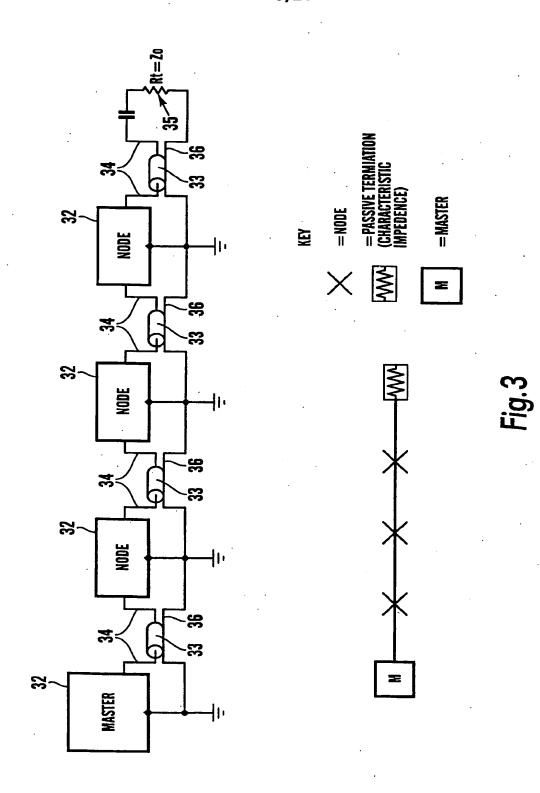


Fig.2



TO NODES

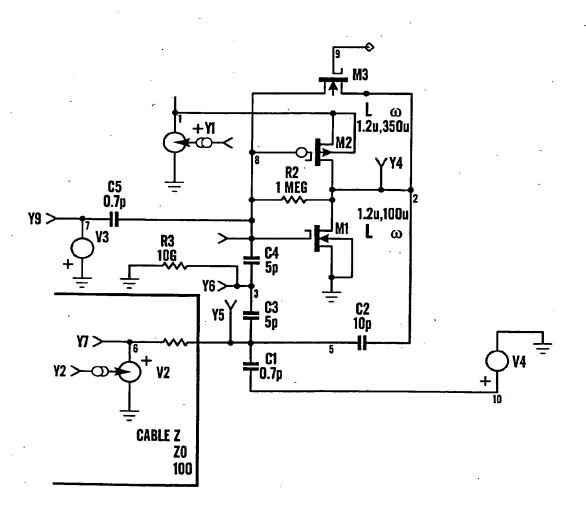
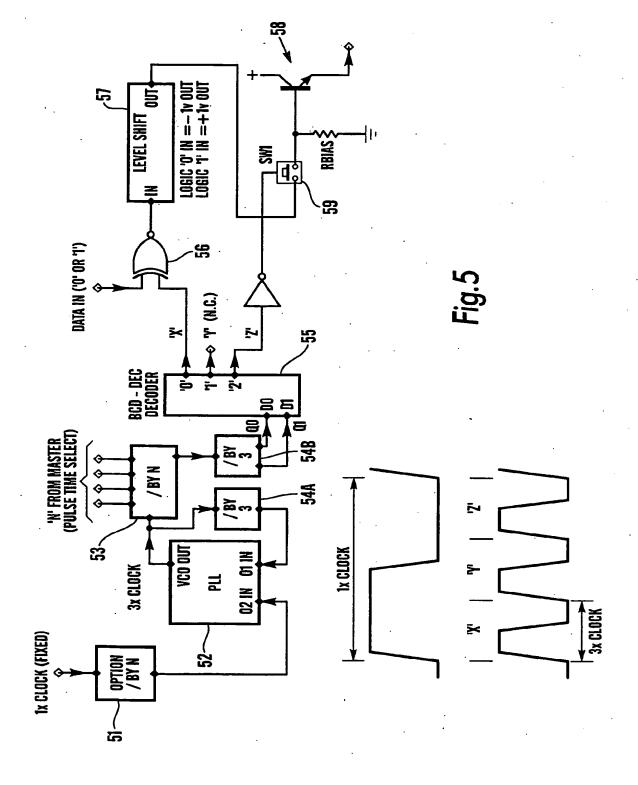
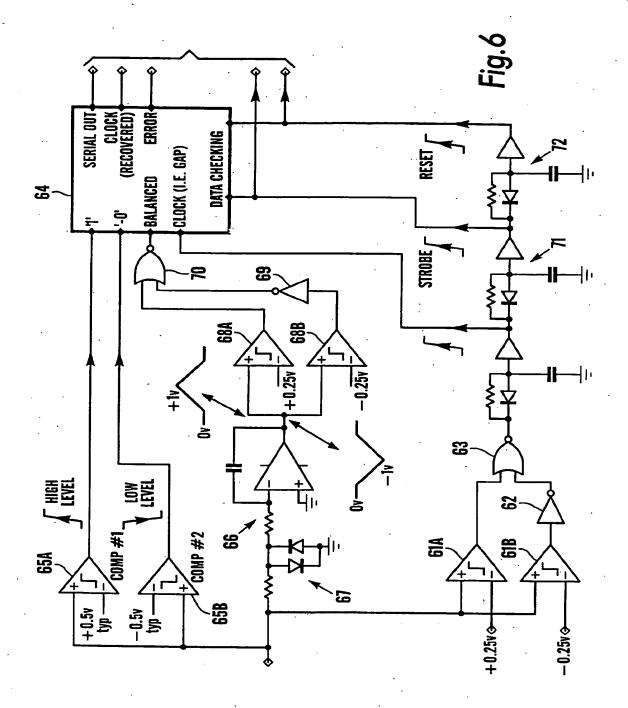
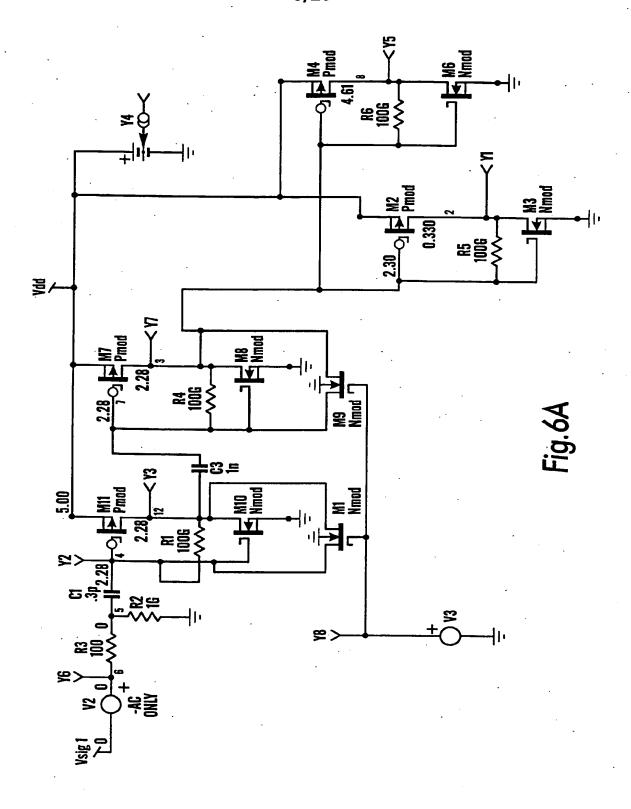


Fig.4A

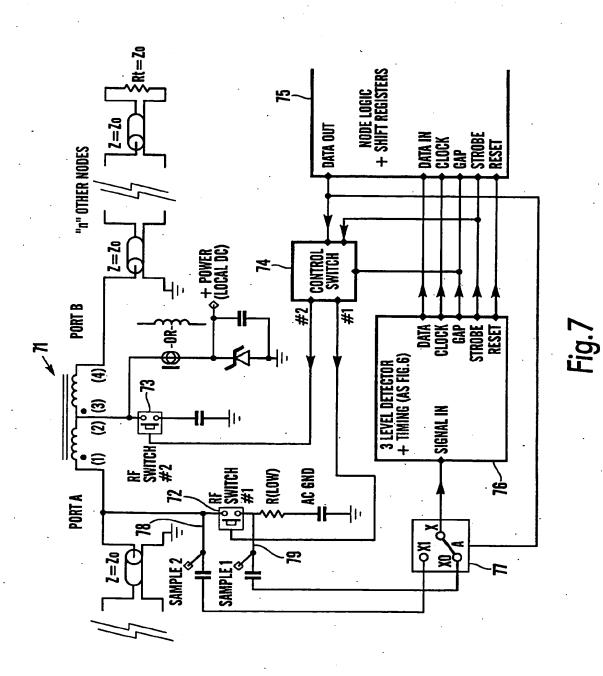


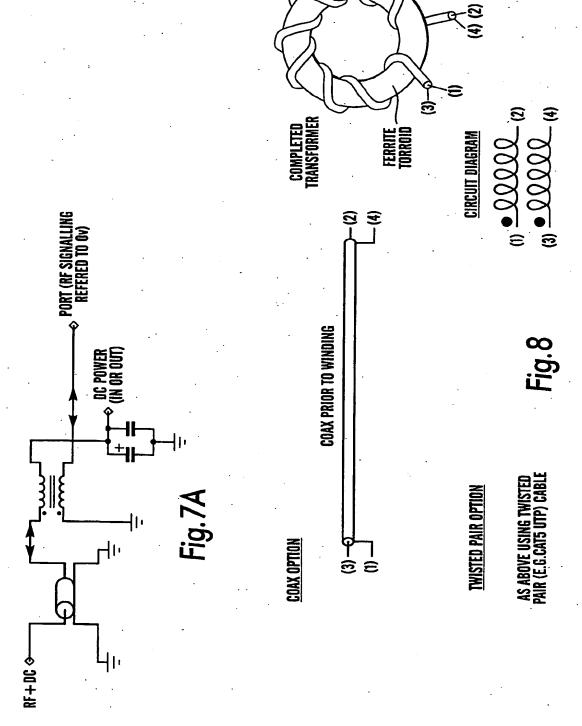
USBLINGS CYLCC





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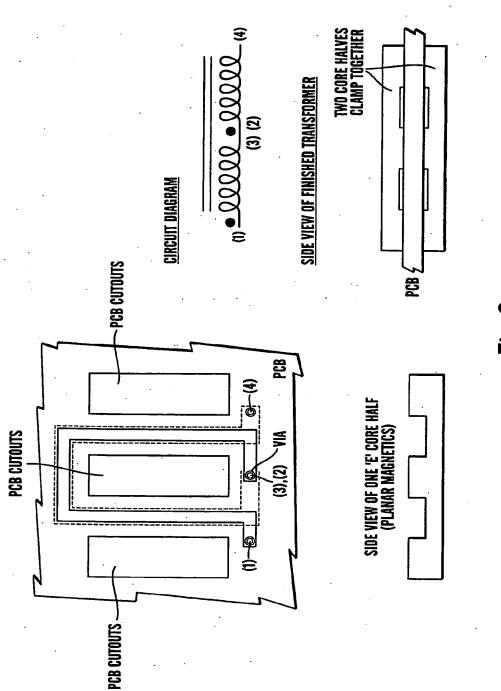


Fig. 9

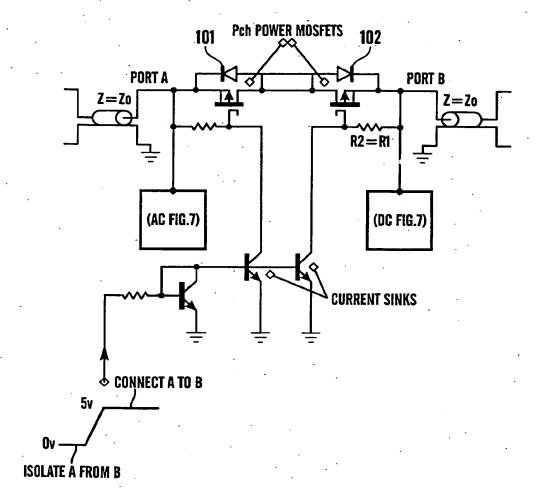
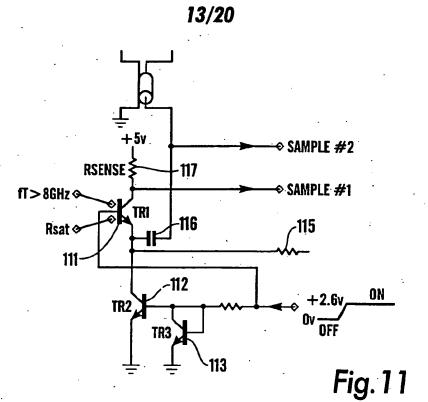
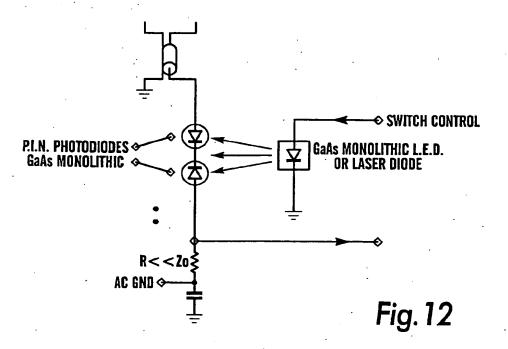


Fig. 10





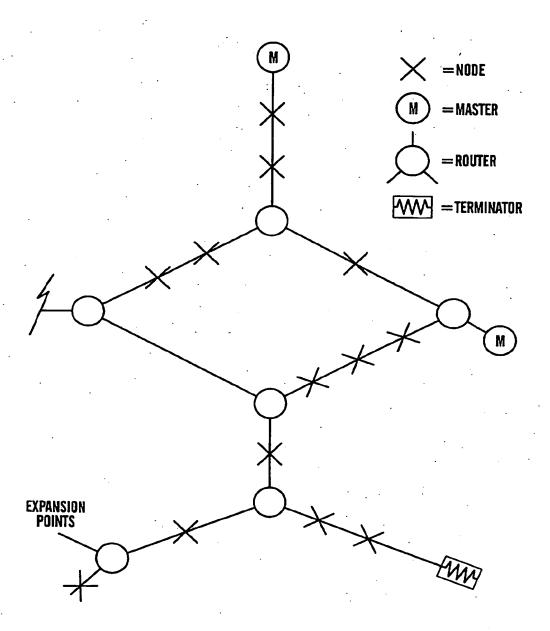
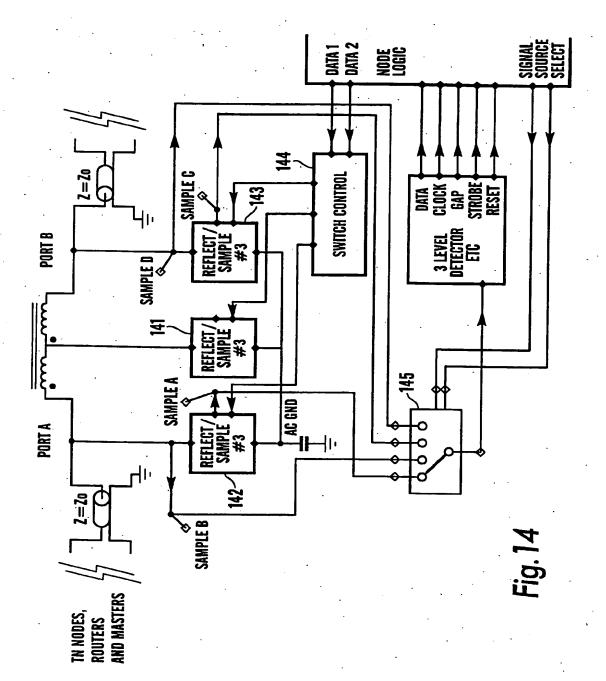
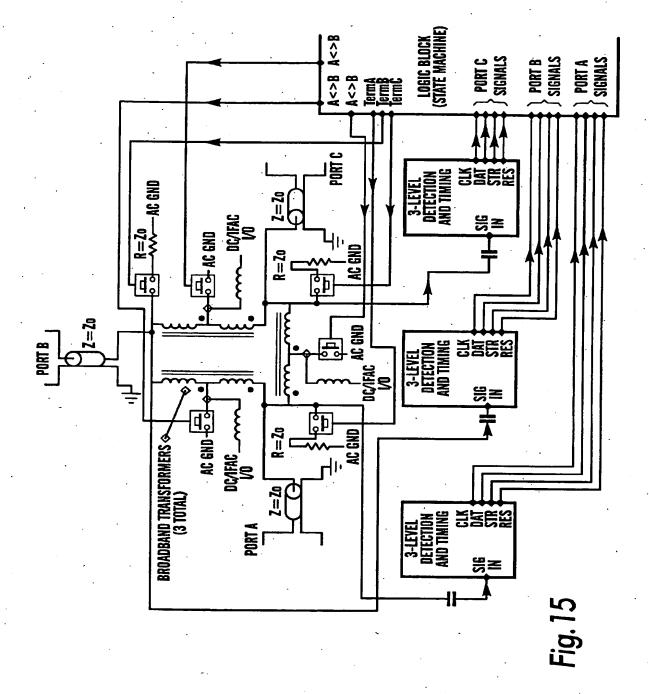


Fig. 13





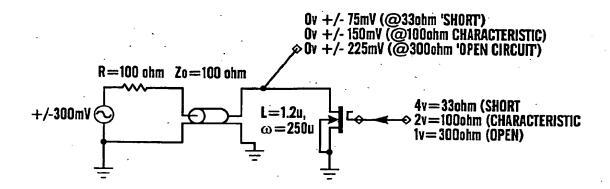


Fig. 15A

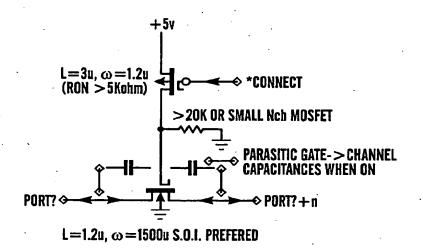
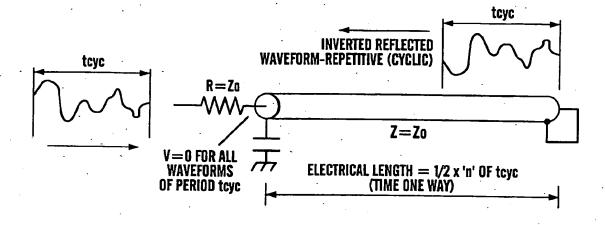


Fig. 15B

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MEMORY EFFECT ON WANTED SIGNALS WHEN THEN COMBINED AT THE COAX ENTRANCE (SPURIOUS SIGNALS HAVING BEEN MOVED)

Fig. 17

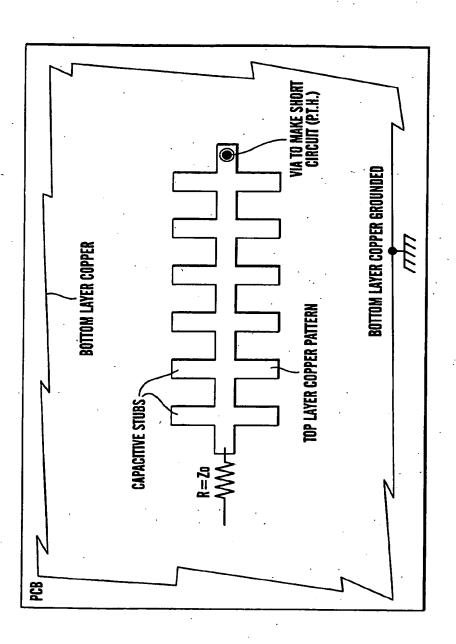


Fig. 18